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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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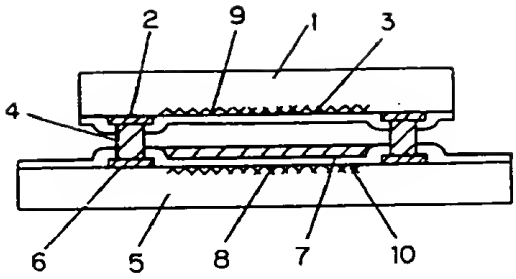
Abstract

Purpose

To provide, for a semiconductor device called a system module in which multiple semiconductor elements have been stacked in layers, a semiconductor device that can reduce the crosstalk between the semiconductor elements.

Constitution

For a semiconductor device in which a first semiconductor element 1 having a first electrode pad 2 and a first wiring layer 9 is stacked on a second semiconductor element 5 having a second electrode pad 6 and a second wiring layer 10, conductive layer 7 is provided on top of insulation layer 8 of the second semiconductor element 5.



Key: 1 First semiconductor element
2 First electrode pad
3 Passivation layer
4 Bump (connecting material)
5 Second semiconductor element
6 Second electrode pad
7 Conductive layer (electroconductive material)
8 Insulation layer (insulating material)
9 First wiring layer
10 Second wiring layer

Claims

1. A semiconductor device provided with a first semiconductor element having a first electrode pad and a first wiring layer on its main surface; a second semiconductor element having a second electrode pad and a second wiring layer on its main surface and arranged facing said first semiconductor element; a connecting material that electrically connects said first electrode pad and said second electrode pad; and insulating material and electroconductive material stacked between said opposing main surfaces of said first semiconductor element and said second semiconductor element.

2. The semiconductor device of Claim 1, wherein the insulating material comprises an insulation layer formed on the main surface of at least one of the first semiconductor element or the second semiconductor element, and the electroconductive material comprises a conductive layer formed on said insulation layer.

3. The semiconductor device of Claim 1, wherein the insulating material comprises an insulation film which provides a connecting material at the periphery, and the electroconductive material comprises a conductive layer that is formed on at least one of the surfaces of said insulation film.

4. The semiconductor device of Claim 1, wherein the insulating material comprises an insulating resin, and the electroconductive material comprises a conductive case embedded in said insulating resin.

5. The semiconductor device of Claim 1, 2, 3, or 4, wherein the connecting material comprises a metal protrusion.

6. The semiconductor device of Claim 1, 2, 3, or 4, wherein the electroconductive material is connected to the ground terminal of the first semiconductor element and/or the second semiconductor element and/or an external circuit.

7. Manufacturing method for a semiconductor device that includes: a step in which the main surfaces of a first semiconductor element having a first electrode pad and a first wiring layer on its main surface and a second semiconductor element having a second electrode pad and a second wiring layer on its main surface are arranged facing one another; a step in which an insulating material and an electroconductive material are arranged in a stack between said two opposing main surfaces of said first semiconductor element and said second semiconductor

element; and a step in which said first electrode pad and said second electrode pad are electrically connected by means of a connecting material.

8 The manufacturing method for a semiconductor device of Claim 7, wherein the step in which the insulation layer is arranged comprises a step in which an insulation layer is formed on the wiring layer of the first semiconductor element and/or the second semiconductor element, and the step in which the electroconductive material is arranged comprises a step in which a conductive layer is formed on said insulation layer.

9. The manufacturing method for a semiconductor device of Claim 7, wherein the step in which a connection is made comprises a step in which the connection is made by means of a protruding electrode that is formed on both sides of an insulation film; the step in which the electroconductive material is arranged comprises a step in which a conductive layer is formed for at least one surface of said insulation film on at least the region where said protruding electrode is not formed; and the step in which the insulating material is arranged includes a step in which an insulating resin is applied to the first semiconductor element, a step in which said insulation film is placed on said insulating resin such that the first electrode pad and said protruding electrode as well as the second electrode pad and said protruding electrode oppose one another, and a step in which an insulating resin is then applied on top of said insulation film.

10. The manufacturing method for a semiconductor device of Claim 7, wherein the step in which an insulating material is arranged as well as the step in which an electroconductive material is arranged comprise a step in which an insulating resin is applied on top of the first semiconductor element; a step in

which a conductive case is placed in the region on said insulating resin other than where the first electrode pad portion is formed; and a step in which insulating resin is applied to the top of said insulating case and said insulating case is embedded in said insulating resin.

11. The manufacturing method for a semiconductor device of Claim 7 or 8, wherein the step in which the electroconductive material is arranged is a step in which said electroconductive material is formed by an electroless plating method.

12. The manufacturing method for a semiconductor device of Claim 7, 8, 9, or 10, which includes a step in which the electroconductive material is connected to the ground terminal of at least one of the first semiconductor element, the second semiconductor element, or an external circuit.

13. A semiconductor device provided with a first semiconductor element having a first electrode pad and a first wiring layer and a first element region on its main surface; and a second semiconductor element having a second electrode pad and a second wiring layer and a second element region on its main surface and arranged to face said first semiconductor element; and the surface area of said second semiconductor element is greater than that of said first semiconductor element; and said second wiring layer as well as said second element region are formed at a location that is separated from the location where said first wiring layer and said first element region are stacked on top of said second semiconductor element.

14. The semiconductor device of Claim 13, wherein a memory is formed in the second element region that is capabale of being erased as well as rewritten by means of infrared irradiation.

15. The semiconductor device of Claim 13, wherein the number of second electrode pads is greater than the number of first electrode pads; furthermore, the surface area of the second element region is smaller than the surface area that results when the total surface area of the first wiring layer and the first element region is subtracted from the surface area of the second semiconductor element.

16. A semiconductor device provided with a first semiconductor element having a first electrode pad and a first wiring layer and a first element region on its main surface, and a second semiconductor element having a second electrode pad and a second wiring layer and a second element region on its main surface and arranged to face said first semiconductor element; and said first semiconductor element and said second semiconductor element are arranged in a configuration such that the wiring of said first wiring layer and the wiring of said second wiring layer are not in contact, and wherein they may intersect at any given angle.

17. A semiconductor device provided with a first semiconductor element having a first electrode pad and a first wiring layer and a first element region on its main surface, and a second semiconductor element having a second electrode pad and a second wiring layer and a second element region on its main

surface and arranged to face said first semiconductor element; and the difference between the activation voltage of the first semiconductor element and the activation voltage of the second semiconductor element is smaller than the threshold voltage that turns on or off the semiconductor element that has the lower activation voltage.

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